What is claimed is:

1. A hybrid content addressable memory array comprising:

a first memory portion having a first type of content addressable memory cells arranged in rows and columns;

a second memory portion having a second type of content addressable memory cells arranged in rows and columns, the second type of content addressable memory cells being electrically coupled to the first type of content addressable memory cells.

2. The hybrid content addressable memory array of claim 1, wherein the first memory portion and the second memory portion include matchlines, each matchline of the first memory portion being coupled to the first type of content addressable memory cells, and each matchline of the second memory portion being coupled to the second type of content addressable memory cells.

3. The hybrid content addressable memory array of claim 2, wherein the first type of content addressable memory cells include ternary content addressable memory cells and the second type of content addressable memory cells include binary content addressable memory cells.

4. The hybrid content addressable memory array of claim 3, wherein the matchlines of the first memory portion and the matchlines of the second memory portion are interleaved with each other.

5. The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells include binary content addressable memory cells.

6. The hybrid content addressable memory array of claim 1, wherein the second type of content addressable memory cells include ternary content addressable memory cells.

7. The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells include SRAM based binary content addressable memory cells.

8. The hybrid content addressable memory array of claim 1, wherein the second type of content addressable memory cells include SRAM based ternary content addressable memory cells.

9. The hybrid content addressable memory array of claim 1, wherein at least one of the first and the second type of content addressable memory cells include configurable ternary-binary content addressable memory cells.

10. The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells and the second type of content addressable memory cells of a row are coupled to a logical matchline.

11. The hybrid content addressable memory array of claim 10, wherein the logical matchline includes a segmented matchline.

12. The hybrid content addressable memory array of claim 11, wherein the segmented matchline includes a first matchline segment and a second matchline segment.

13. The hybrid content addressable memory array of claim 12, wherein the first type of content addressable memory cells are coupled to the first matchline segment and the second type of content addressable memory cells are coupled to the second matchline segment.

14. The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells and the second type of content addressable memory cells of a column are coupled to common searchlines.

15. A hybrid content addressable memory array comprising:

a first type of content addressable memory cells coupled to a logical matchline; and

a second type of content addressable memory cells coupled to the logical matchline.

16. The hybrid content addressable memory array of claim 15, wherein the first type of content addressable memory cells include binary content addressable memory cells and the second type of content addressable memory cells include ternary content addressable memory cells.

17. The hybrid content addressable memory array of claim 16, wherein the binary content addressable memory cells include SRAM based binary content addressable memory cells and the ternary content addressable memory cells include SRAM based ternary content addressable memory cells.

18. The hybrid content addressable memory array of claim 15, wherein the logical matchline includes a segmented matchline.

19. The hybrid content addressable memory array of claim 18, wherein the segmented matchline includes at least two matchline segments.

20. The hybrid content addressable memory array of claim 19, wherein the first type of content addressable memory cells are coupled to one of the at least two matchline segments and the second type of content addressable memory cells are coupled to the other of the at least two matchline segments.

21. A hybrid content addressable memory array comprising:

a first type of content addressable memory cells coupled to common searchlines; and

a second type of content addressable memory cells coupled to the common searchlines.

22. The hybrid content addressable memory array of claim 21, wherein the first type of content addressable memory cells include binary content addressable memory cells and the second type of content addressable memory cells include ternary content addressable memory cells.

23. The hybrid content addressable memory array of claim 22, wherein the binary content addressable memory cells include SRAM based binary content addressable memory cells and the ternary content addressable memory cells include SRAM based ternary content addressable memory cells.